We have amended claims 1 and 13 to specify planarization of an intermediate layer to a specified roughness level. As explained on page 9, lines 4-5 of the specification, flattening the surface to the specified degree results in "high quality material ... well suited for state of the art CMOS processing."

We submit that neither cited reference discloses or even suggests planarization, or the benefits of the recited roughness level to CMOS devices and processing techniques.

Accordingly, we submit that all claims are now in condition for allowance.

Please charge any fee occasioned by this paper to our Deposit Account No. 20-0531.

Respectfully submitted,

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Reg. No. 33,497

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MARKED-UP COPY OF CLAIMS AS AMENDED

1. (Amended) A method of fabricating a CMOS inverter comprising:

providing a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure comprising a planarized surface located between the strained surface layer and the Si substrate and having a surface roughness less than 1 nm; and

integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

~~2. The method of claim 1, wherein the heterostructure further comprises a planarized surface positioned between the strained surface layer and the Si substrate.~~

~~3. The method of claim 1, wherein the surface roughness of the strained surface layer is less than 1nm.~~

13. (Amended) A method of fabricating an integrated circuit comprising:

providing a heterostructure having a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained layer on said relaxed $Si_{1-x}Ge_x$ layer; ~~and~~

planarizing a surface between the strained layer and the Si substrate to a surface roughness less than 1 nm; and

forming a p transistor and an n transistor in said heterostructure, wherein said strained layer comprises the channel of said n transistor and said p transistor, and said n transistor and said p transistor are interconnected in a CMOS circuit.

~~14. The method of claim 13, wherein the heterostructure further comprises a planarized surface positioned between the strained layer and the Si substrate.~~

~~15. The method of claim 13, wherein the surface roughness of the strained layer is less than 1nm.~~